1. A hybrid magnetoelectronic spin-based memory cell comprising:

an electron spin-based memory element situated on a silicon based substrate; said electron spin-based memory element including:

i) a first ferromagnetic layer with a changeable magnetization state;

ii) a second ferromagnetic layer with a non-changeable magnetization state;

iii) a base layer which is less than 1 micron in thickness and is situated between said first ferromagnetic layer and said second ferromagnetic layer, said base layer comprising a material having electron levels that are not significantly affected by an electron spin;

a memory cell selector coupled to said electron spin-based memory element, said memory cell selector including a semiconductor based transistor isolation element also situated on said silicon based substrate.

2. The hybrid magnetoelectronic spin-based memory cell of claim 1, wherein said electron spin-based memory element is situated on top of said semiconductor based FET and separated by an insulation layer.

3. The hybrid magnetoelectronic spin-based memory cell of claim 1, wherein an impedance of the electron spin-based memory element is on the order of 1 ohm.

4. The hybrid magnetoelectronic spin-based memory cell of claim 1 wherein a spin transimpedance increases as said electron spin-based memory element decreases in size.

5. The hybrid magnetoelectronic spin-based memory cell of claim 1 wherein a resistance of said base layer is the same or larger than a transimpedance of said electron spin-based memory element.

6. The hybrid magnetoelectronic spin-based memory cell of claim 1, wherein said memory cell selector is coupled to a bit line, and further including a second semiconductor based transistor isolation element coupling said electron spin-based memory element to a bit reference line.

7. The hybrid magnetoelectronic spin-based memory cell of claim 1 wherein the semiconductor based transistor isolation element is a field effect transistor (FET).

8. The hybrid magnetoelectronic spin-based memory cell of claim 1 wherein the semiconductor based transistor isolation element is a bipolar junction transistor (BJT).

9. The hybrid magnetoelectronic spin-based memory cell of claim 1, further including a read line coupled to read data from said electron spin-based memory element, and a separate write line coupled to write data to said electron spin-based memory element.

10. The hybrid magnetoelectronic spin-based memory cell of claim 9, wherein said write line uses a single polarity current pulse.

11. The hybrid magnetoelectronic spin-based memory cell of claim 1, wherein said write line includes two partially overlapping write lines.

12. The hybrid magnetoelectronic spin-based memory cell of claim 11, wherein said electron spin-based memory element only changes state when a current pulse is present on both of said two overlapping write lines.

13. The hybrid magnetoelectronic spin-based memory cell of claim 1, wherein said electron spin-based memory element is a spin transistor.

14. The hybrid magnetoelectronic spin-based memory cell of claim 1, wherein said base layer is grounded.

15. The hybrid magnetoelectronic spin-based memory cell of claim 1, wherein both a current pulse and a voltage pulse are used to read data stored by said electron spin-based memory element.

16. A hybrid magnetoelectronic spin-based memory cell comprising:

an electron spin-based memory element situated on a silicon based substrate; said electron spin-based memory element including:

i) a first ferromagnetic layer with a first changeable magnetization state comprising permalloy and/or cobalt;

ii) a second ferromagnetic layer with a second non-changeable magnetization state also comprising permalloy and/or cobalt;

iii) a conductive paramagnetic base layer which is less than 1 micron in thickness and is situated between said first ferromagnetic layer and said second ferromagnetic layer, said base layer comprising a paramagnetic material capable of passing a spin polarized current;

a memory cell selector coupled to said electron spin-based memory, said memory cell selector including a semiconductor based isolation element.

17. The hybrid magnetoelectronic spin-based memory cell of claim 16, wherein said electron spin-based memory element is stacked on top of a second electron spin-based memory element.

18. The hybrid magnetoelectronic spin-based memory cell of claim 16, wherein said electron spin-based memory element and said second electron spin-based memory element share said memory cell selector.

19. The hybrid magnetoelectronic spin-based memory cell of claim 16, wherein said electron spin-based memory element is a three terminal, current biased device.

20. The hybrid magnetoelectronic spin-based memory cell of claim 16, wherein said conductive paramagnetic base layer is adapted to create a nonequilibrium population of spin polarized electrons and an equivalent nonequilibrium magnetization M.

21. The hybrid magnetoelectronic spin-based memory cell of claim 20, wherein said nonequilibrium magnetization M in said paramagnetic conductive paramagnetic base layer base generates an electric field at an interface with said first ferromagnetic layer.

22. The hybrid magnetoelectronic spin-based memory cell of claim 16, wherein said spin polarized current has an amplitude that varies based on whether said first changeable magnetization state and said second non-changeable magnetization state are parallel or antiparallel.

23. A hybrid magnetoelectronic spin-based memory cell comprising:

an electron spin-based memory element situated on a silicon based substrate; said electron spin-based memory element including:

i) a first ferromagnetic layer with a changeable magnetization state comprising permalloy and/or cobalt;

ii) a second ferromagnetic layer with a non-changeable magnetization state also comprising permalloy and/or cobalt;

iii) a base layer which is less than 1 micron in thickness and is situated between said first ferromagnetic layer and said second ferromagnetic layer, said base layer comprising an aluminum based material capable of carrying a spin polarized current;

wherein said base layer further includes a low transmission barrier interface to said first ferromagnetic layer;

a memory cell selector coupled to said electron spin-based memory, said memory cell selector including a semiconductor based isolation element.

24. The hybrid magnetoelectronic spin-based memory cell of claim 23, further including a second low transmission barrier interface associated with said second ferromagnetic layer.

25. The hybrid magnetoelectronic spin-based memory cell of claim 23 wherein said second ferromagnetic layer is a bilayer including both a first ferromagnetic conductor layer and a second nonmagnetic conductor layer, which second nonmagnetic conductor layer is used to control a magnetic behavior of said first ferromagnetic conductor layer.

26. The hybrid magnetoelectronic spin-based memory cell of claim 23, further including a read line coupled to read data from said electron spin-based memory element, and a separate write line coupled to write data to said electron spin-based memory element.